IN THE SPECIFICATION

Please amend the paragraph on page 1, lines 5-7 as follows:

This application is a Continuation-in-part of U.S. Patent Application Ser. No. 09/827,029, filed on April 5, 2001[[;]] , and claims benefit of U.S. Provisional Patent Application Ser. No. 60/226,856, filed on August 22, 2000. U.S. Patent Application Ser. No. 09/827,029 is a Continuation of U.S. Patent 6,233,389, filed on July 30, 1998.

Please amend page 5, line 33-page 6, line 2, as follows:

Figs. 19A and 19B are [[is]] a block diagram of a first embodiment of the system of Figure 14 according to the invention;

Figs. 20A and 20B are [[is]] a block schematic diagram of a second embodiment of the system of Figure 14 according to the invention;

Figs. 21A and 21B are [[is]] a block schematic diagram of a third embodiment of the system of Figure 14 according to the invention; and

Please amend the paragraph on page 23, line 33-page 24, line 6 as follows:

The MPEG-2 encoder 1604 accepts input from the NTSC/PAL/SECAM video decoder 1602 and the audio input previously mentioned and produces an MPEG-2 transport stream as the output. In the preferred embodiment of the invention, the encoder 1604 is programmed to multiplex the audio and video inputs into a constant bitrate (CBR) MPEG-2 transport stream. However, in order to conserve disk space, it is also possible to program the encoder 1604 to produce a variable bit rate (VBR) stream. Subsequently, the transport stream is delivered to the decoder 1404 over the transport interface 1406 for demultiplexing and further processing. The input section 1401a further includes a memory element 1605 that is not under the control of the OS kernel. Figures 19A and 19B provide[[s]] a block schematic diagram of a system board 1900 incorporating the input section 1401a and the output section 1402. As shown, the MPEG-2 encoder is connected to the MPEG-2 decoder/graphics subassembly 1404 as a client on the PCI bus 1407.

Please amend the paragraph on page 24, lines 13-21 as follows:

Turning now to Figure 17, an input section 1401b is shown adapted to accept a digital satellite signal. The digital satellite input section 1401b accepts input from dual satellite

receivers 1701. Demodulators 1702 demodulate the incoming QPSK (quadrature phase shift keying) to yield a transport stream. Because the satellite transport stream is not fully MPEG-2 compliant, the MPEG-2 decoder/graphics subassembly 1404 must have the capability of decoding either type of stream. Thus, the transport stream is passed to the output section 1402 via the transport interface 1406 without any further modification or processing. Figures 20Aand 20B provide[[s]] a block diagram of a system board 2000 incorporating the input section 1401b.

Please amend the paragraph on page 24, line 23-page 25, line 2 as follows:

Referring to Figure 18, an input section 1401c designed to accept either digital or analog cable input is shown. The input section accepts input from one or more RF coaxial connectors 1801, 1802 in both digital and analog format. The analog portion functions similarly to that of the analog input section 1401a. The video signal is decoded by dual NTSC decoders 1602. The audio is processed by dual multi-standard sound processors 1603 and the resulting output is fed to dual MPEG-2 encoders. It should be noted that, in the current version of the input section, each component is provided in duplicate. The digital cable signal is routed to dual demodulators 1803. Depending on the cable signal modulation, the demodulators may be either or both of QAM (quadrature amplitude modulation) and QPSK, either with or without DOCSIS (Data Over Cable Service Interface Specification) and/or DAVIC (Digital Audio Visual Council) support. As shown, the digital signal demodulators have associated with them a memory element 1804 that is controlled independently of the OS kernel. Figures 21A and 21B provide[[s]] a block diagram of a system board 2100 incorporating the digital cable input section 1401c. As in the previous versions, transport streams are passed to the output section 1402 via the transport interface 1406. The digital cable input section 1401c is connected to the MPEG-2 decoder/graphics subsection 1404 as a client on the PCI bus.